REMARKS

This is in response to the Office Action mailed January 28, 2004. Applicants respectfully traverse and request reconsideration.

Applicants' Attorney extends gratitude to Examiner Ha for niceties extended during an April 26, 2004 telephone conference. No direct agreement was reached for the allowability of pending claims, although the interpretation of the term "system memory" was discussed. The Examiner indicated that a broad interpretation of the limitation processor interface as inherently containing memory which would be equivalent to the claimed system memory, to which Applicants continue to traverse.

Election/Restriction

In the previous response, Applicants provisionally elected Group I, claims 1-16 for examination in response to the Examiner's Restriction/Election requirement. Therefore, Applicants have explicitly withdrawn claims 17-20. Therefore the present Restriction/Election requirement is met and is in proper form for allowance.

Rejection of claims under 35 U.S.C. § 102

Claims 1-4, 9-12 and 16 currently stand rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 6,346,946 ("Jeddeloh"). Applicants submit the present rejection is improper because Jeddeloh fails to disclose all of the claimed limitations.

In support of the present rejection, the Examiner has indicated that the claimed system memory of the present invention is disclosed by Jeddeloh as the processor interface 126. Applicants respectfully disagree and submit that the processor interface 126 of Jeddeloh is what it is described to be, an interface including circuitry for communicating with processors attached to a processor bus 108. *See* col. 4, lines 21-23. As noted above, during the telephone interview with the Examiner, the Examiner indicated that the processor interface 126 would inherently contain memory which discloses the system memory, to which Applicants disagree.

Looking initially at the claim limitation of system memory, claims 1 and 10 have been amended to provide further clarifying language that the system memory is operative to store system instructions. Moreover, a dictionary definition of system memory includes "read/write memory accessible by both the processor and the I/O unit in the system address base. It is usually thought of as being in one or more third party nodes, but could alternatively by wholly or partially located in the communicating processor or I/O nodes." *See* IEEE Authoritative Dictionary of IEEE Standard Terms, 7th Ed.

The IEEE Authoritative Dictionary of IEEE Standard Terms further provides multiple definitions of the term "interface." Most applicable, the term interface is defined as "a shared electrical boundary between parts of a computer system, through which information is conveyed." The McGraw-Hill Telecom Dictionary, 4th Ed. defines the term "interface" to be "a device or software program that connects two separate entities. The two entities can be virtual (software), hardware/electronic devices, or distinguish a separation of responsibility between two parties (telephone network interface)." The American Heritage Dictionary, 3rd Ed. defines interface as a surface forming a common boundary between adjacent regions, bodies, substances or phases. A point in which independent systems or diverse groups interact. The point of interaction or communication between a computer and any other entity, such as a printer."

Applicants respectfully submit that the Examiner has improperly interpreted of the term "interface" with respect to the processor interface 126 of Jeddeloh. The Examiner's interpretation is not only beyond the plain and ordinary meaning of the term interface as defined by the specification of Jeddeloh which is silent as to a specific definition of a processor interface other than its ordinary meaning. For example, as used in col. 3, lines 23-24 Jeddeloh states "processor interface 126 for communicating with processor bus 108." Furthermore, the Examiner has provided an interpretation beyond the dictionary definition of the term interface as noted by three exemplary dictionary definitions quoted above. While Applicants appreciate the Examiner's broad interpretation of the interface inherently containing memory, Applicants submit that the Examiner is improper in asserting this as disclosing the claimed limitation of system memory as claimed in claims 1 and 10. Claims 1 and 10 recite the system memory

operative to store system instructions and the system instructions may be stored and retrieved from the system memory.

Even assuming *arguendo* that the interface 126 of Jeddeloh does include some type of temporary memory for interfacing, this would not constitute the claim system memory of claims 1 and 10 and it is not operative to store system instructions but is only operative to store transient data in an interface setting, which is inconsistent with the claimed present invention.

More specifically, the system of Jeddeloh operates in a completely different manner which is providing a specific interface between the north bridge 102 and processor 112-116 across the processor bus 108 and produces a completely different result which is having system memory located outside of the north bridge which would require further processing delay for getting information across the processor bus. In other words, Jeddeloh describes specifically the prior art approach to which the present invention overcomes because, among other things, the processor interface does not contain the claimed system memory of the present invention but only provides for interfacing with the processors 112-116 across the processor bus 108 for access through the switch 124 as described in the corresponding specification of Jeddeloh.

Therefore, Applicants respectfully request reconsideration and withdrawal of the present invention. Should the Examiner maintain the present rejection, Applicants request a showing, including specific column and line numbers, of the exact delineation of where the processor interface 126 of Jeddeloh discloses including memory constituting the system memory, as claimed in the present invention. In the alternative, Applicants request further support of the Examiner's position of the inherency of memory within the processor interface 126 and support for the inherent memory to constitute the claimed system memory of the present invention. Regarding claims 2-4, 9 and 11-12, Applicants respectfully resubmit the above position offered with regards to claims 1 and 10 respectively and submit that these claims contain further patentable subject limitations therein. It is further submitted these claims are allowable not merely as being dependent upon an allowable base claim. But rather, Jeddeloh fails to disclose all of the claimed limitations including, but not limited to, the system memory disposed within

the integrated circuit of the present invention. Therefore, reconsideration and withdrawal of the present rejection is respectfully requested.

Rejection of claims under 35 U.S.C. § 103(a)

Claims 5-8 and 13-16 currently stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jeddeloh in view of U.S. Patent Application No. 2003/0183934 ("Barrett").

Regarding claims 5-8 and 13-16, Applicants respectfully resubmit the above position offered with regards to claims 1 and 10 respectively and submit these claims contain further limitations thereof. It is further submitted these claims contain patentable subject matter and are allowable not merely as being dependent upon an allowable base claim. But rather, the combination of Jeddeloh and Barrett fails to teach or suggest, among other things, the claimed system memory disposed within the integrated circuit of the present invention. Therefore, reconsideration and withdrawal is respectfully requested.

Accordingly, Applicant respectfully submits that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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